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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/058,946	GODA ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	MW

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) *19-47* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5, 10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 1-18 in Paper No. 8 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation of "....wherein upper surfaces of the first shallow trench isolation regions are formed into *convex* shapes ..." must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 1, 10, 11 and 16 are objected to because of the following informalities.

Claims 1 and 11 recite "...said pair of source and drain regions using a surface of the semiconductor substrate sandwiched therebetween as a channel..." Understanding is that the source and the drain are *using* (?) the recited the substrate region as a channel. Actually, a channel is formed between the source and the drain when the device operates.

Claim 10 recites "...the gate electrode is a continuous film without interposition of a natural oxide film *therein*." Does this imply that there is no interposition of a natural oxide film *in* the gate electrode?

Claim 16 recites "... impurities of a first conductivity type are doped in a first number of the *first gate electrode* out of the plurality of the first gate electrodes..., ... impurities of a first conductivity type are doped in a first number of the *second gate electrode* out of the plurality of the second gate ..., ... impurities of a second conductivity type are doped in a second number of the *first gate electrodes*... , ... impurities of a second conductivity type are doped in a second number of the *second gate electrodes*..." There is not a clear indication for what these numbers imply and the reciting the first number in a singular gate and the second number in plural gates is very confusing.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8, 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara (US 6301155) in view of Park et al. (US 6326268), hereafter Park.

Regarding claim 1, Fig. 3 of Fujiwara shows a semiconductor device comprising:

a semiconductor substrate (101);

shallow trench isolation regions (102) formed in the semiconductor substrate;

a pair of source and drain regions (S, D) formed in the semiconductor substrate, said pair of source and drain regions using a surface of the semiconductor substrate sandwiched therebetween as a channel;

a gate insulating film (6 in Fig. 4) formed on the semiconductor substrate and a gate electrode (8 in Fig.4; a floating gate and a control gate) formed on the gate insulating film.

Fujiwara shows substantially the entire claimed structure except that the thickness of the gate insulating film at a central portion of the channel and at portions contacting with the shallow trench isolation regions are equal. Fig. 7 of Park shows the insulating layers (30) are formed without a curvature or without bending at the edges contacting the isolation trench (22; col. 3, lines 52-58). It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the teaching of Park into the device of Fujiwara to have the thickness of the gate insulating film equal at a central portion of the channel and at portions contacting with the shallow trench isolation regions in order to minimize the charge leakage path (col. 3, lines 17-25).

Regarding claim 2, Fig. 4 of Fujiwara shows the gate insulating film includes:

a first insulating film (12) comprised of silicon and nitrogen as main constituent elements thereof; and

a second insulating film (14) formed on the first insulating film, said second insulating film being different from the first insulating film in main constituent elements.

Fujiwara shows substantially the entire claimed structure except that the thickness of the gate insulating film at a central portion of the channel and at portions contacting with the shallow

trench isolation regions are equal. Fig. 7 of Park shows the insulating layer (48) is formed without a curvature or without bending at the edges contacting the isolation trench (22; col. 3, lines 52-58). The motivation to combine the teachings of Fujiwara and Park has been discussed above in claim 1.

Regarding claim 3, Fig. 4 of Fujiwara shows the gate insulating film includes:

a first insulating film (12) comprised of silicon and nitrogen as main constituent elements thereof; and

a third insulating film (10) formed under the first insulating film and on the semiconductor substrate, said third insulating film being different from the first insulating film in main constituent elements.

Fujiwara shows substantially the entire claimed structure except that the thickness of the gate insulating film at a central portion of the channel and at portions contacting with the shallow trench isolation regions are equal. Fig. 7 of Park shows the insulating layer (44) is formed without a curvature or without bending at the edges contacting the isolation trench (22; col. 3, lines 52-58). The motivation to combine the teachings of Fujiwara and Park has been discussed above in claim 1.

Regarding claim 4, Fig. 4 of Fujiwara shows the gate insulating film includes:

a first insulating film (12) comprised of silicon and nitrogen as main constituent elements thereof;

a second insulating film formed on the first insulating film, said second insulating film being different from the first insulating film in main constituent elements; and

a third insulating film (10)formed under the first insulating film and on the semiconductor substrate, said

third insulating film being different from the first insulating film in main constituent elements.

Fujiwara shows substantially the entire claimed structure except that the thickness of the gate insulating film at a central portion of the channel and at portions contacting with the shallow trench isolation regions are equal. Fig. 7 of Park shows two insulating layer (44, 46) are formed without a curvature or without bending at the edges contacting the isolation trench (22; col. 3, lines 52-58). The motivation to combine the teachings of Fujiwara and Park has been discussed above in claim 1.

Regarding claim 5, Fig. 3 of Fujiwara shows the gate electrode (the control gate; col. 3, lines 38-48) is formed on the shallow trench isolation regions without interposition of the first insulating film.

Regarding claims 6 and 7, Fig. 3 of Fujiwara shows a width of a portion of the semiconductor substrate, the portion being sandwiched between the shallow trench isolation regions, is not more than a width of a portion of the gate electrode (or the first insulating film), the portion being sandwiched between the shallow trench isolation regions.

Regarding claim 8, Fig. 4 of Fujiwara shows a width of the first insulating film in a direction of the channel is equal to a width of the gate electrode in the direction of the channel.

Regarding claim 11, Fig. 3 of Fujiwara shows a plurality of semiconductor devices comprising:

a semiconductor substrate (101);

a first shallow trench isolation regions (102) in the semiconductor substrate;

a first pair of source and drain regions (S,D) formed in the semiconductor substrate, a first channel between said first pair of source and drain regions;

a first gate insulating film (10, 12, 14 in Fig. 4) formed on the semiconductor substrate

a first gate electrode (a floating gate and a control gate) formed on the first gate insulating film.

Fig. 3 of Fujiwara clearly shows a plurality of the semiconductor devices and each of the semiconductor devices with the source and the drain are separated by the isolation region (102). Therefore it is inherent that a plurality of the isolation regions are formed to insulate the devices from each other.

Fujiwara shows substantially the entire claimed structure except that the thickness of the gate insulating film at a central portion of the channel and at portions contacting with the shallow trench isolation regions are equal. Fig. 7 of Park shows the insulating layers (30) are formed without a curvature or without bending at the edges contacting the isolation trench (22; col. 3, lines 52-58). It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the teaching of Park into the device of Fujiwara to have the thickness of the gate insulating film equal at a central portion of the channel and at portions contacting with the shallow trench isolation regions in order to minimize the charge leakage path (col. 3, lines 17-25).

Regarding claim 17, Fig. 3 of Fujiwara shows film thickness of the first gate electrode is equal to film thickness of the second gate electrodes.

Claims 9, 10, 15, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara and Park as applied to claim 5 above, and further in view of Taniguchi et al. (US 6509742), hereafter Taniguchi.

Regarding claim 9, the combined teachings of Fujiwara and Park show substantially the entire claimed structure except "the gate electrode contains impurities, and an impurity concentration of the gate electrode at a portion contacting with the gate insulating film is equal to an impurity concentration thereof at portions contacting with upper planes of the shallow trench isolation regions." Fig 9 of Taniguchi shows an impurity-doped polysilicon gate (7). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Taniguchi into the gate of Fujiwara and Park in order to reduce resistance formed on the principal surface of the substrate (col. 19, lines 30-34).

Regarding the aspect in which the impurity concentration of the gate electrode is equal at the portion contacting with the gate insulating film and at portions contacting with upper planes of the shallow trench isolation regions, it would be obvious that the impurity concentration of the gate electrode would be constant at the contacting portions of the gate insulating layer and the upper surfaces of the shallow trench isolation regions since the impurity is introduced on the continuous gate layer.

Regarding claim 10, the combined teachings of Fujiwara and Park show substantially the entire claimed structure except "the gate electrode is made of polycrystalline silicon containing impurities, and the gate electrode is a continuous film without interposition of a natural oxide film therein." Fig. 17 of Taniguci shows an impurity-doped gate (9a, 9b, 9c) without oxide layer in-between. It would have been obvious to one of ordinary skill in the art at the time of the

invention to incorporate the teaching of Taniguchi into the gate of Fujiwara and Park in order to form peripheral regions of the device of a MOS needed for a variable configuration.

Regarding claim 15, the combined teachings of Fujiwara and Park show substantially the entire claimed structure except "the first gate electrode and the second gate electrode are made of polycrystalline silicon films, which are doped with impurities of conductivity types opposite to each other." Fig. 17 of Taniguchi shows two gates (9a, 9b) with the opposite conductivity (col. 22, lines 3-4; col. 22, lines 52-55). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Taniguchi into the gate of Fujiwara and Park to have a complementary device of a PMOS and an NMOS in order to operate at a low power consumption.

Regarding claim 16, the combined teachings of Fujiwara and Park show substantially the entire claimed structure except a memory section having two different gates and a peripheral section having two different types of devices. Fig. 1 of Taniguchi shows a semiconductor device wherein a memory cell is formed with a floating gate and a control gate while a peripheral regions with a PMOS and an NMOS. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Taniguchi into the device configuration of Fujiwara and Park to form a memory cell and a CMOS circuit on one chip (col. 1, lines 12-15).

Regarding claim 18, the combined teachings of Fujiwara and Park show substantially the entire claimed structure except "the peripheral circuit section includes peripheral circuit transistors." Fig. 1 of Taniguchi shows a semiconductor device with a peripheral circuit region (high and low withstand voltage regions). It would have been obvious to one of ordinary skill in

the art at the time of the invention to incorporate the teaching of Taniguchi into the device configuration of Fujiwara and Park to form a peripheral circuit section to perform an additionally required function.

Note that Fig. 1 of Fujiwara shows an selected cells which have constitutions of the gate electrodes and the gate insulating films, the constitutions being identical to constitutions of the gate electrodes and the gate insulating films of the memory transistors as shown in Fig. 3.

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara and Park as applied to claim 11 above, and further in view of Yu et al. (US 6376877), hereafter Yu.

Regarding claim 12, the combined teachings of Fujiwara and Park show substantially the entire claimed structure except "the first shallow trench isolation regions and the second shallow trench isolation regions have concave portions on upper ends individually thereof, and depths of the concave portions provided on the first
shallow trench isolation regions are smaller than depths of the concave portions provided on the second shallow trench isolation regions." Fig. 7A of Yu shows a concave portions on upper ends of the shallow trench isolation regions in a memory device. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Yu into the shallow trench isolation regions of Fujiwara and Park in order to reduce semiconductor device geometry.

Regarding the aspect of the difference in the concave portions in the first and the second shallow trench isolation regions, it would have been an obvious matter of design choice to have the depths of the concave portions on the first shallow trench isolation regions smaller than

depths of the concave portions on the second shallow trench isolation regions since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Regarding claim 13, the combined teachings of Fujiwara and Park show substantially the entire claimed structure except "upper surfaces of the first shallow trench isolation regions are formed into convex shapes, and the second shallow trench isolation regions have concave portions on upper ends thereof." 7B of Yu shows a memory device wherein upper surfaces of the first shallow trench isolation regions are formed into convex shapes, and the second shallow trench isolation regions have concave portions on upper ends. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Yu into the shallow trench isolation regions of Fujiwara and Park to accommodate the design need. In addition, a modification would have involved a mere change in the shape of a component. A change in shape is generally recognized as being within the level of ordinary skill in the art. In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara and Park as applied to claim 11 above, and further in view of Satoh et al. (US 6531350), hereafter Satoh.

Regarding claim 14, the combined teachings of Fujiwara and Park show substantially the entire claimed structure except "the second gate insulating film is a silicon oxide film excluding nitrogen as a main constituent element." Fig. 1A of Satoh shows the second gate insulating film

(120 underneath 141) is a silicon oxide film without nitrogen (col. 6, lines 38-39). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Satoh into the second gate insulating film of Fujiwara and Park to form a MOS device for a memory configuration suitable for various architectures.

Note that Fig. 4 of Fujiwara shows the first gate insulating film includes:

a first insulating film (12) comprised of silicon and nitrogen as main constituent elements thereof;

a second insulating film (14)formed on the first insulating film, said second insulating film being different from the first insulating film in main constituent element; and

a third insulating film (10) formed under the first insulating film and on the semiconductor substrate, said third insulating film being different from the first insulating film in main constituent elements, and the second gate insulating film is a silicon oxide film excluding nitrogen as a main constituent element.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (703) 305-3998. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (703) 308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmi
November 17, 2003

EDDIE LEE
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